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**STI White Paper: AN092309R1**

**Reduce your MEMS Package Level Final Test Times and Save MEMS Manufacturing Costs using STI3000 Dynamic Wafer Level Test Technology**

## Introduction

A survey of MEMS manufacturing literature indicates that packaging and test costs are typically 80% of the total product cost. [Examples: 1, 2, 3]. One of the major constraints in MEMS manufacturing is the package testing. Package level testing is a high cost manufacturing constrain that is driven by long calibration and final test times. This paper will describe how dynamic wafer level testing is be used to reduce the package level calibration and final test times and result in an increase in throughput of package testing and reduce the overall MEMS manufacturing costs for capacitive MEMS products.

## Background

MEMS wafer fabrication processes typically involve etching materials, such as silicon, to produce electrically passive and mechanically active sensor elements that meet a specified performance criteria based on a simulated MEMS design. The MEMS wafer fabrication process is not perfect due to the tolerances associated with the etching process and to the complex geometries inherent in most MEMS designs. Oftentimes, the wafer foundry does not completely understand the variability of their etching process, because there is not a suitable process control monitor or measurement available that represents the final device geometry or device performance across the entire wafer. This process variability results in MEMS wafers that contain devices with a wide distribution of mechanical performance. It is then the purpose of the control chip or ASIC that attaches to the MEMS chip to calibrate this wide performance range into a narrow performance range according to the final product specifications. This can result in long calibration and final test times and poor final test yields that can significantly increase the product and manufacturing costs. One limiting factor in MEMS manufacturing is the inability to measure the dynamic mechanical behavior of the MEMS device at wafer-level. Figure 1 below shows a typical MEMS manufacturing flow using conventional wafer level testing.

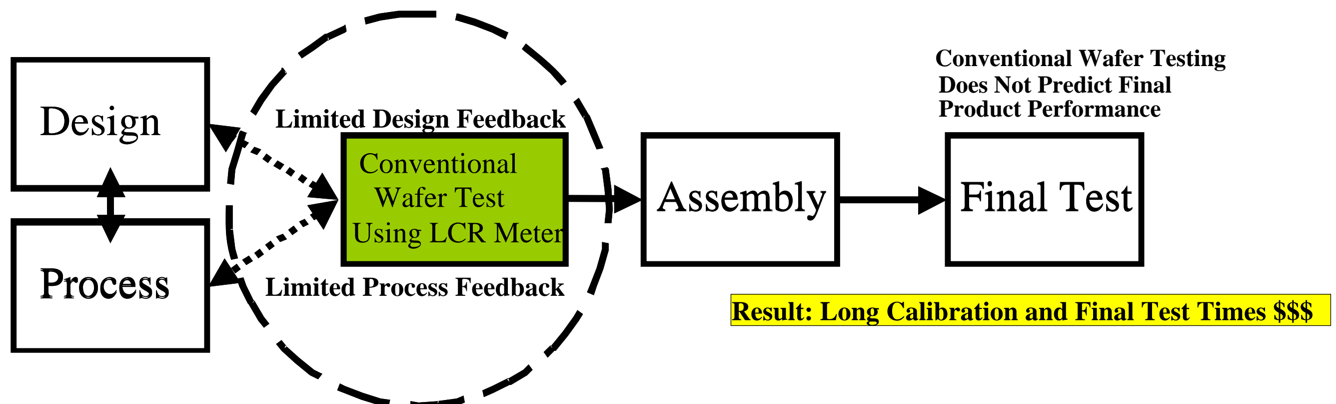


**Figure 1: MEMS Manufacturing Flow using Conventional Wafer Testing**

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**MEMS Wafer Level Conventional Testing**

Conventional MEMS wafer level testing for capacitive sensor elements uses a LCR meter to test the device leakage current and the static capacitance unbiased at 0V and biased with a DC voltage applied. A capacitance to voltage (C-V) curve can then be generated that estimates the device initial capacitance (Farads) and sensitivity (Farads/Volts).

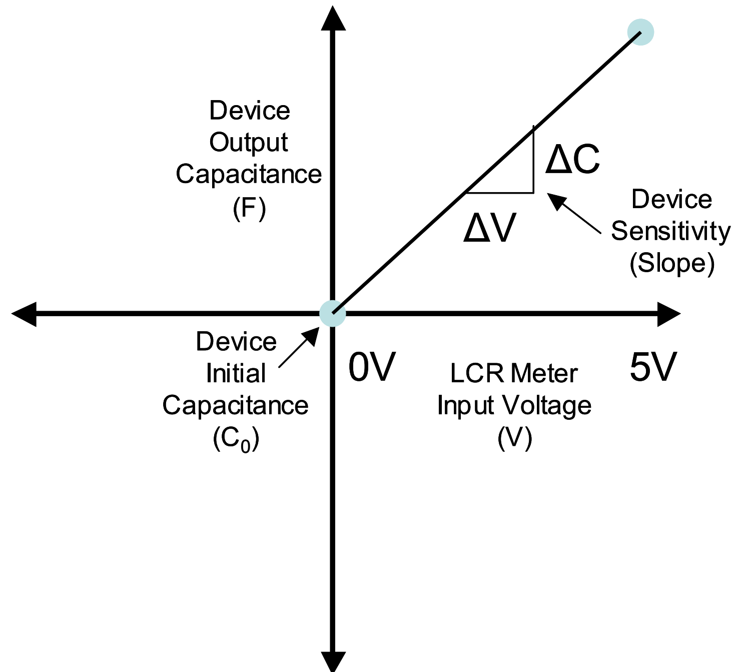


**Figure 2: Wafer-Level Static Capacitance Measurements using LCR Meter**

Although effective for detecting gross device failures, such as broken MEMS structures or stuck MEMS elements, the static DC tests do not predict the device will pass package level calibration or final dynamic testing. For static DC measurements using a LCR meter, a wide distribution of MEMS dynamic AC parameters can go unseen until the devices are packaged and calibrated at final test on a mechanical stimulus test system. The inability to predict final device performance results in longer calibration and final test times, and more failing devices at package level test.

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**MEMS Wafer Level Dynamic Testing using STI3000 Drive Sense Technology**
Solidus Technologies has developed an innovative and unique wafer-level dynamic test equipment technology called the STI3000 (Fig. 4). This technology can test the dynamic mechanical AC performance of the MEMS device before the expensive package level calibration and final test stage. The STI3000 can measure AC performance parameters at wafer level (Fig. 3), including resonant frequency, quality factor (Q), mechanical f3dB frequency, as well as hysteresis and stiction. These AC parameters better represent and predict the true mechanical behavior of the MEMS device [5]. This dynamic performance data can be used to correlate to etching processes, reduce fabrication process variation and increase package-level calibration final test throughput.

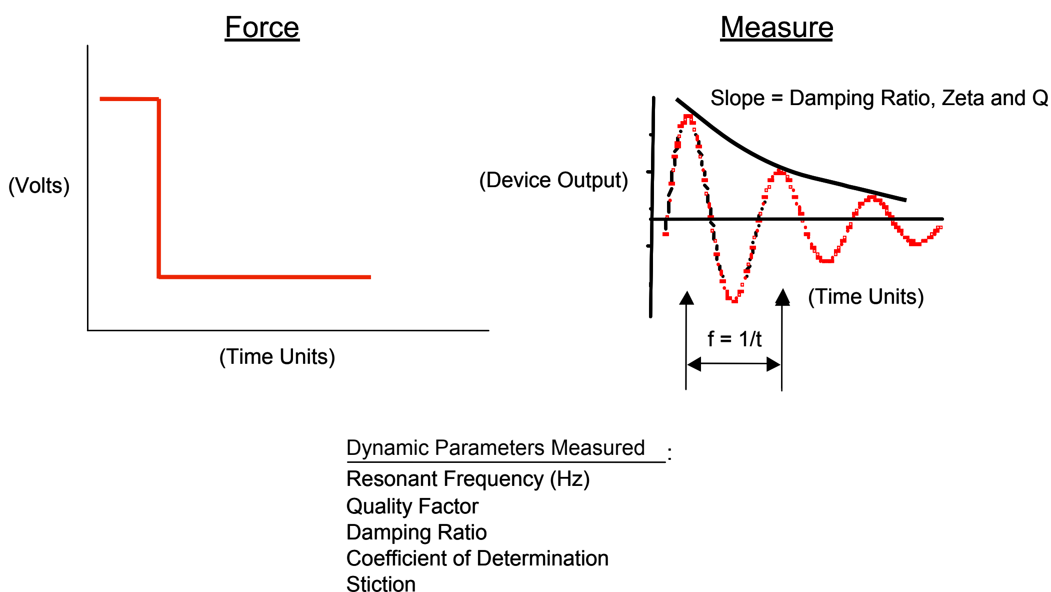


**Figure 3: Wafer-Level "Dynamic"Capacitance Measurements using STI3000**

**Figure 4: STI3000 Test Head Type I Module**

**Comparison of Conventional Static versus Dynamic Wafer Testing**

Table A provides a summary of conventional static versus dynamic wafer testing. Static capacitance testing can be used to detect broken or stuck MEMS elements, but does not provide suitable test data that can be used to improve the fabrication process or to predict final package level device dynamic performance. The static capacitance test time is significantly longer (>50%) than the STI3000 dynamic test times. Dynamic measurements using the STI3000 test system provide higher test coverage to the MEMS sensor element as shown below in Table A. This wafer-level dynamic behavior test data can be used to improve product quality, increase product yields, improve product throughput, resulting in manufacturing cost savings.

**Table A: MEMS Wafer-Level Static versus Dynamic Test Summary**

| Step | Measurement | Type | Purpose / Failure Mode | Estimated Test Time (second/axis) |
|---|---|---|---|---|
| 1 | Static Capacitance | Static | Detecting Broken or Stuck Elements. Provides No value for improving process or product quality. (This test can be replaced by other dynamic tests, such as Pull-in/Release Voltage test) | 3 seconds / axis |
| 2 | Pullin Voltage | Dynamic | Detecting Stiction, Hysteresis, Spring Constant and Stuck Elements | 0.35 second / axis |
| 3 | Release Voltage | Dynamic | Detecting Stiction, Hysteresis, Spring Constant and Stuck Elements | 0.35 second / axis |
| 4 | Resonant Frequency | Dynamic | Determining Damping Characteristics, Detecting Hermeticity of Lid Seal and Validating Etching Process is in Control | 0.2 second / axis |
| 5 | Quality Factor | Dynamic | Determining Damping Characteristics, Detecting Hermeticity of Lid Seal and Validating Etching Process is in Control | |
| 6 | Coefficient of Determination | Dynamic | Statistically validates the resonant frequency, Q and hysteresis measurements by fitting a model to the measured data. | Calculations (Zero Test Time) |
| 7 | Mechanical Hysteresis | Dynamic | Validates Etching Process and Mechanical Properties of MEMS Design. This parameter is measured during the pull-in and release voltage tests | |

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**MEMS Accelerometer Calibration**

"Some 10 to 30 % of standard semiconductor manufacturing costs is driven by final tests. For MEMS, besides the regular ASIC test, the sensor needs to be calibrated, increasing this share even higher"[4]. For a MEMS accelerometer, the calibration of its offset (g) and sensitivity (V/g) parameters is essential to guarantee the product will meet its final product performance requirements (Fig. 5).

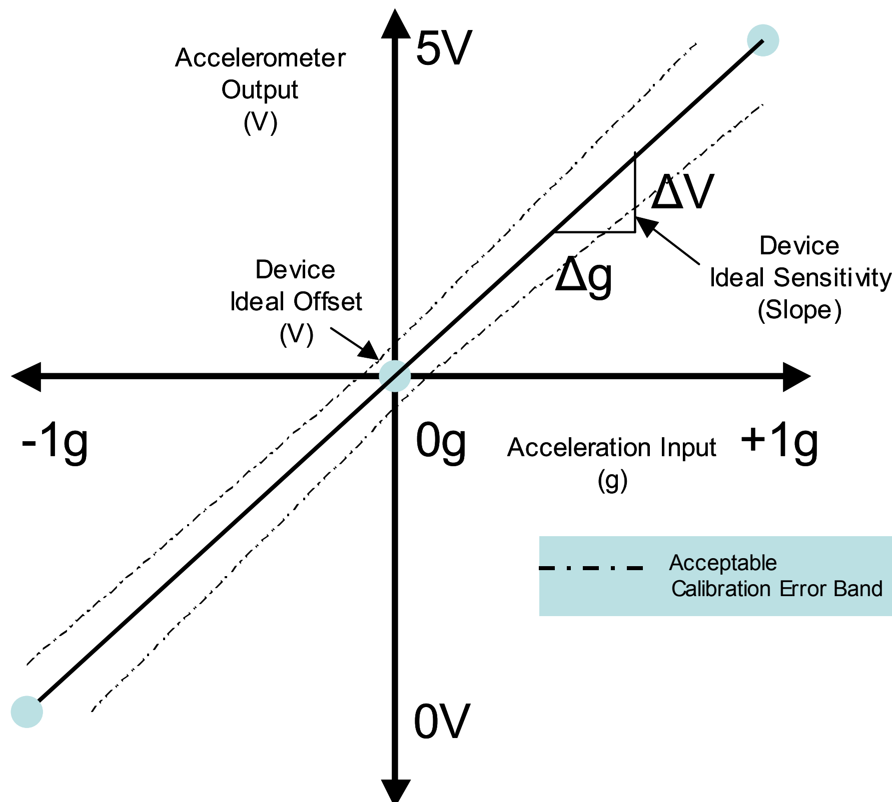


**Figure 5: Calibration Profile for a MEMS Accelerometer**

The calibration process for an accelerometer requires that a mechanical stimulus, such as a shaker or tumble station be used to apply changes in g-force to the accelerometer while the ASIC is determining the number of calibration iterations (i.e. DAC voltage steps) required to calibrate the device within specification. If the mechanical dynamic performance distribution (i.e. Spring Rate) of MEMS devices prior to calibration is wide then there will be an associated wide distribution of calibration test times associated with the number of iterations required to calibrate the device within specification, which increases test time and product cost.

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**Case Study: Reducing MEMS Calibration Test Times for a MEMS Accelerometer**

A single axis MEMS accelerometer was manufactured through two different manufacturing flows (Fig. 6). One flow used conventional wafer testing and the other used dynamic wafer testing.

The conventional wafer test used a LCR meter that tested the accelerometer leakage, and static capacitance biased and unbiased. Over 90% of the devices passed the conventional wafer level testing. As shown below, the devices that passed conventional wafer testing had a large distribution of calibration and final package test times, which produced an average calibration time of 3 seconds per device and an average verification test time of 1.5 seconds per device for an average total package level test time of 4.5 seconds per device.

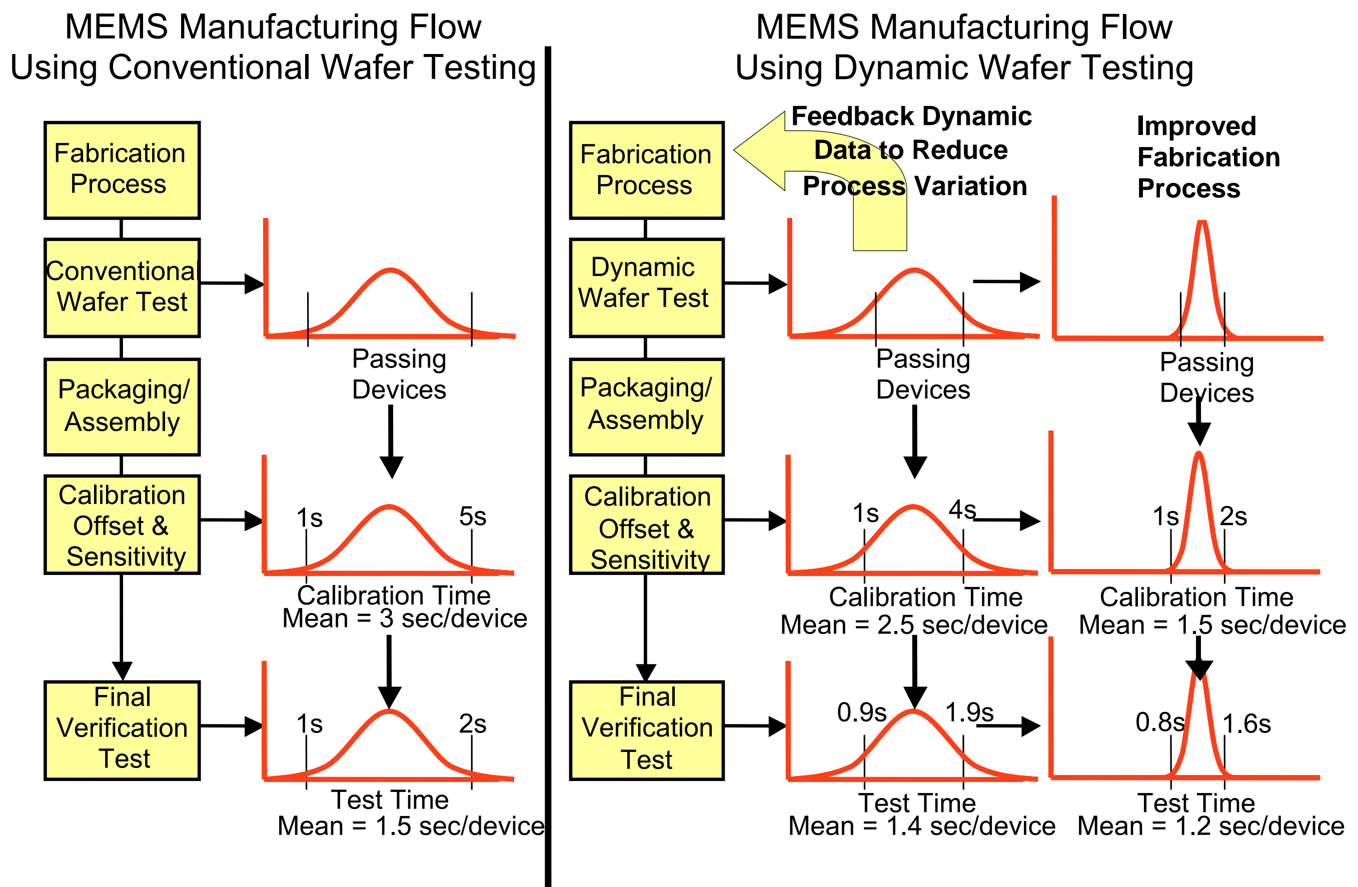


**Figure 6: Calibration and Final Test Time Reduction using Dynamic Wafer Testing**

The dynamic wafer test used the STI3000 test system, which tested the accelerometer leakage, f3dB frequency, resonant frequency, quality factor and stiction. Approximately 80% of the devices passed the dynamic wafer level testing. As shown in Figure 6, the devices that passed dynamic wafer testing had a reduced distribution of calibration test times, which produced an average calibration test time of 2.5 seconds per device and an average verification test time of 1.4 seconds per device for an average total package level test time of 3.9 seconds per device. This resulted in a savings of 0.6 sec/device or 13.3% improvement in final package testing (UPH).

The dynamic wafer level test distributions were then analyzed and a correlation was established with the accelerometer beam width and the accelerometer wafer-level resonant frequency measurement. These correlations led to a determination of the DRIE beam width etch resolution. Based on this correlation, process changes were made to the DRIE process step and process control monitors and new test limits were established on the STI3000 for the resonant frequency parameter. This resulted in a narrow distribution of wafer-level dynamic performance parameters. As shown in Figure 7, the devices that passed dynamic wafer testing with the improved process had a reduced distribution of calibration test times, and produced an average calibration test time of 1.5 seconds per device and an average verification test time of 1.2 seconds per device for an average total package level test time of 2.7 seconds per device. This resulted in a throughput savings of 1.8 sec/device or 40% improvement in final package test costs (Table B).

**Table B: Accelerometer Calibration and Final Test Time Comparison**

| **Package-Level Test Flow** | **Test Times using Conventional Wafer Test** | **Test Times using Dynamic Wafer Test** | **Test Time Savings using Dynamic Wafer Test** |
|---|---|---|---|
| Calibration<br>-Offset<br>-Sensitivity | 3 sec/device | 1.5 sec/device | 1.5 sec/device |
| Final Verification Test<br>-Leakage<br>-Supply Current<br>-Offset<br>-Selftest<br>-Sensitivity<br>-Linearity<br>-f3dB Frequency | 1.5 sec/device | 1.2 sec/device | 0.3 sec/device |
| **Total Package-Level Calibration and Final Test Time Savings using STI 3000 Dynamic Wafer Test** | | | **1.8 sec/device (40% increased UPH)** |

## Conclusion

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MEMS package level calibration and final test times are a major contributor to the reduction of throughput and increased cost of a MEMS device. Identifying this constraint and transferring it earlier in the manufacturing process can save significant product and manufacturing costs. The STI3000 test system has demonstrated the ability to reduce this calibration and final test time by at least 40% for a single axis MEMS accelerometer, resulting in a significant MEMS product cost savings. The STI3000 dynamic wafer testing will produce even more cost savings for tri-axis accelerometers, gyroscopes and inertial measurement units, where package level calibration and test times are more expensive.

The need for final package level test cost reductions is becoming more apparent as the MEMS commercial market and volumes are exploding. The STI3000 innovative dynamic wafer test technology has been a missing link in the MEMS manufacturing process that will allow MEMS manufacturers to reduce their overall product development and manufacturing costs.

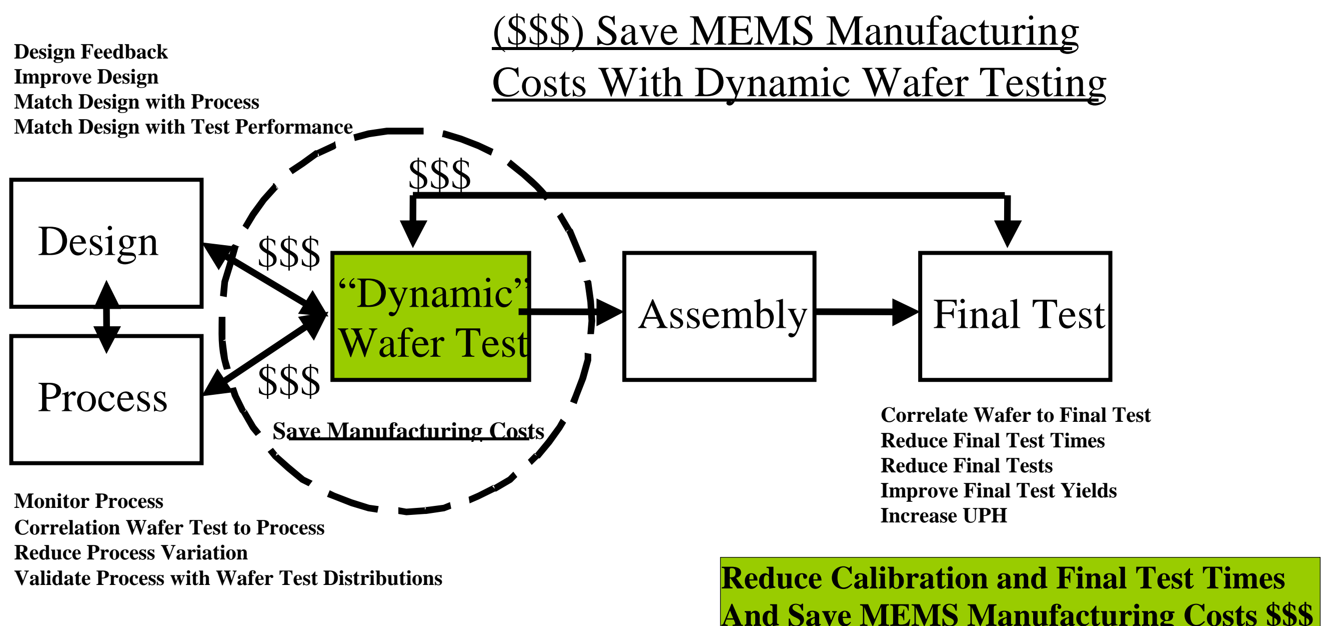


**Figure 7: MEMS Manufacturing Flow using "Dynamic" Wafer Testing**

**References**

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**[2] Yole Developpement "Status of the MEMS Industry" September 2008**

**[3] Steven Nasiri "Wafer-Scale Packaging and Integration Are Credited for** New Generation of Low-Cost MEMS Motion Sensor Products" July 2007

**[4] Andreas Nagy "The new final test" October 2006**

**[5] John Rychcik "A Better Test for MEMS Inertial Sensors" March 2006**

**See Also**

**STI3000 Wafer Probe System**
**http://www.solidustech.com/STI3000WaferProbeTestSystem.html**

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**http://www.solidustech.com**